UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/586,525	06/02/2000	Ying-Chou Tsai	JCLA5827	6171

7590 12/30/2002

J C Patents Inc
4 Venture
Suite 250
Irvine, CA 92618

EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/586,525	Applicant(s) TSAI ET AL.	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-7 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lach et al. (6,108,212).

Lach et al. teach in figure 1 a substrate structure of flip chip package comprising a plurality of patterned circuit layer 22 connected by vias 30, at least an insulative layer 14 stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of the flip chip package as a top patterned circuit layer, and the top patterned circuit layer comprises at least a plurality of first mounting pads 27 and plurality of a second mounting pads 26 (figures 6, 8) and a solder mask layer 42 (figure 2) covering the patterned circuit layer on the surface of the substrate of the flip chip package, the solder mask layer partially covering a first top surface of the first mounting pads 27 while entirely exposing a second top surface and sidewalls of the first mounting pads 26 and the whole surface

of the second mounting pad, wherein the first mounting pads 27 are disposed at a periphery region of the substrate (figure 1), and a chip 12 having an active surface with a plurality of bumps 64 disposed thereon wherein the chip has its active surface face to the surface of the substrate 14 of the flip chip package, and the bumps are electrically connected to their corresponding first bonding pads and second bonding pads respectively and an underfill material filling between the active surface of the chip and the top surface of the substrate of the flip chip package, wherein the bumps attach only to the top surface of the first mounting pads.

Although Lach et al. do not state that the first mounting pads 27 are disposed on the periphery region of the substrate, figure 1 depicts first mounting pads 27 are disposed at the edge of the substrate. Therefore, the first mounting pads 27 are disposed on the periphery region of the substrate, as claimed.

The embodiment of figure 1 of Lach et al. does not depict second mounting pads disposed at a central region of the substrate. Lach et al. teach in the embodiment of figures 6 and 8 a plurality of second mounting pads 26 disposed at a central region of the substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the second mounting pads at a central region of the substrate, as depicted in the layout of figures 6 and 8, in Lach et al.'s device, in order to reduce the electrical resonances and reflections of the device and to increase the circuit density of the device. The combination is motivated by the teachings of Lach

et al. who point out the advantages of using the layout depicted in figures 6 and 8 (column 2, lines 26-55). Note that the broad recitation of the claim does not require that all the first mounting pads are disposed on the periphery region of the substrate and all the second mounting pads are disposed at a central region of the substrate.

3. Claims 2-4, 8-10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lach et al. in view of Admitted Prior Art (APA).

Lach et al. teach substantially the entire claimed structure, as applied to claims 1 and 7 above, except bumps attach to both the top surface and side surfaces of the second mounting pads.

APA teaches in figure 2 a BT substrate structure of flip chip package wherein each of the patterned circuit layer is formed by a copper foil layer defined by photo lithographic and etching processes, and bumps attach to both the top surface and side surfaces of the second mounting pads (pages 1-2).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to attach bumps to both the top surface and side surfaces of the second mounting pads in Lach et al.'s device in order to increase the contact area between the bumps and the second mounting pads.

Regarding claims 4 and 10, APA teaches that the pitch of the first mounting pads is smaller than the pitch of the second mounting pad (pages 2-3). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the pitch of the first mounting pads smaller than the pitch of the second mounting pad in Lach et al.'s device in order to reduce the size of the device.

4. Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lach et al. and APA, as applied to claims 1 and 7 above, and further in view of Katchmar (6,194,782).

Lach et al. and APA teach substantially the entire claimed structure, as applied to claims 1 and 7 above, except the pitch of the first mounting pads being smaller than the pitch of the second mounting pad.

Katchmar teaches in figure 5 the pitch of the first mounting pads (of bumps 40) is smaller than the pitch of the second mounting pad (of bumps 24). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the pitch of the first mounting pads smaller than the pitch of the second mounting pad in Lach et al. and APA's device in order to reduce the size of the device.

Response to Arguments

5. Applicant argues on page 6 that Lach et al. do not teach any patterned circuit layers in the substrate.

Lach et al. teach in figure 1 patterned circuit layers 22 formed in the substrate.

6. Applicant argues on page 6 that Lach et al. do not teach a solder mask layer covering the top patterned circuit layer on the top surface of the substrate.

Applicant recites in claim 1 a top patterned circuit layer comprises at least a plurality of first mounting pads. Lach et al. teach in figure 1 a solder mask layer 42 covering the at least a plurality of first mounting pads 27. Therefore, Lach et al. teach a solder mask layer covering the top patterned circuit layer on the top surface of the substrate, as argued.

7. Applicant argues on pages 6 and 7 that figures 6 and 8 of Lach et al. do not depict a solder mask layer covering the top patterned circuit layer on the top surface of the substrate.

Figures 6 and 8 of Lach et al. are planar views of the mounting pads. The solder mask layer is not depicted in figures 6 and 8 in order to illustrate the locations of

the mounting pads. Clearly, a solder mask layer covers part of the first mounting pads, as depicted in figures 1 and 2.

8. Applicant argues on page 7 that an artisan would understand that "periphery region" means a region of the substrate that is out of the "central region" of the substrate.

The examiner agrees that an artisan would understand that "periphery region" means a region of the substrate that is out of the "central region" of the substrate. That is, a "periphery region" is related to, and external to the "central region". Figures 6 and 8 depict an inner region which can be characterized as a "central region", and a region that is out of the "central region", which can be characterized as "periphery region". Note again that the broad recitation of the claim does not require that all the first mounting pads are disposed on the periphery region of the substrate and all the second mounting pads are disposed at a central region of the substrate.

9. Applicant argues on page 7 that Lach et al. form conductive bumps attached to the top surface of the pads, and this means that Lach et al. is not concerned about good bonding of the conductive bumps to the pads.

Although Lach et al. attach conductive bumps to the top surface of the pads, Lach et al. still teach the claimed limitations as recited in claims 1 and 7.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
December 27, 2002

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800